

FIG. 1

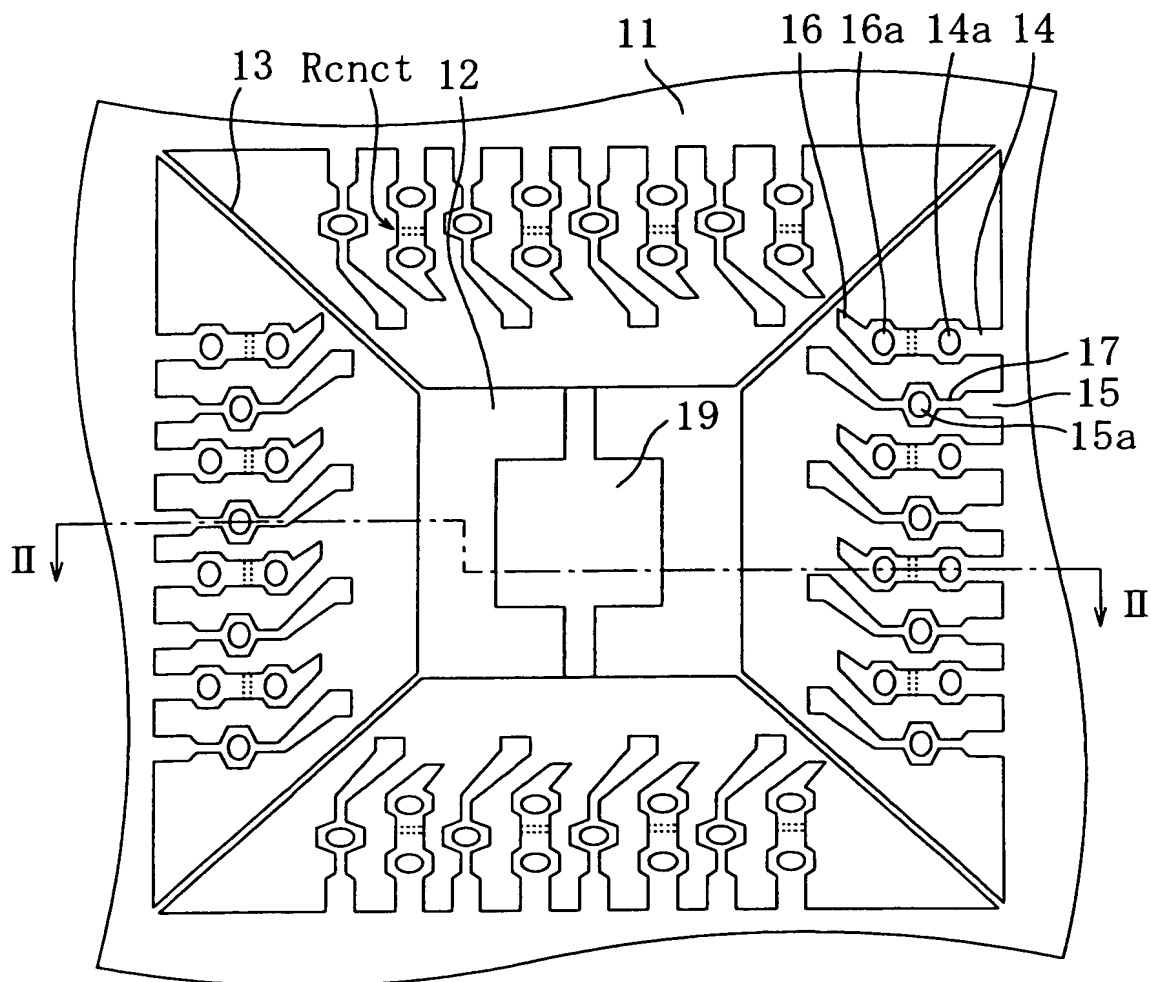


FIG. 2

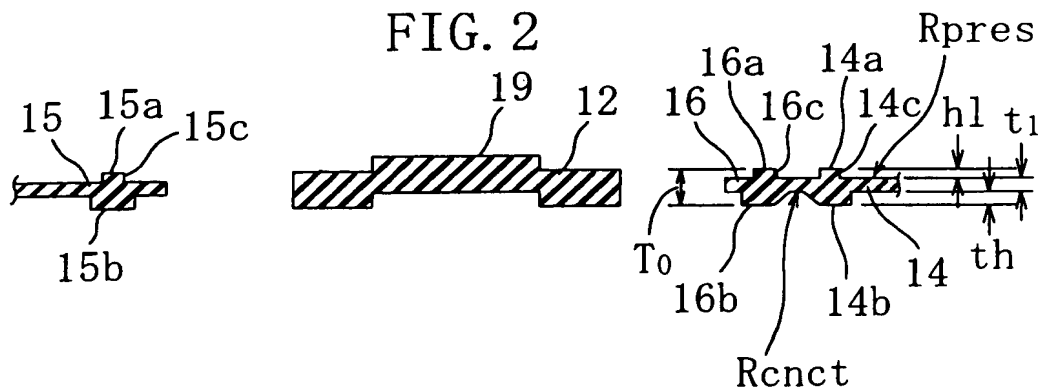




FIG. 3A

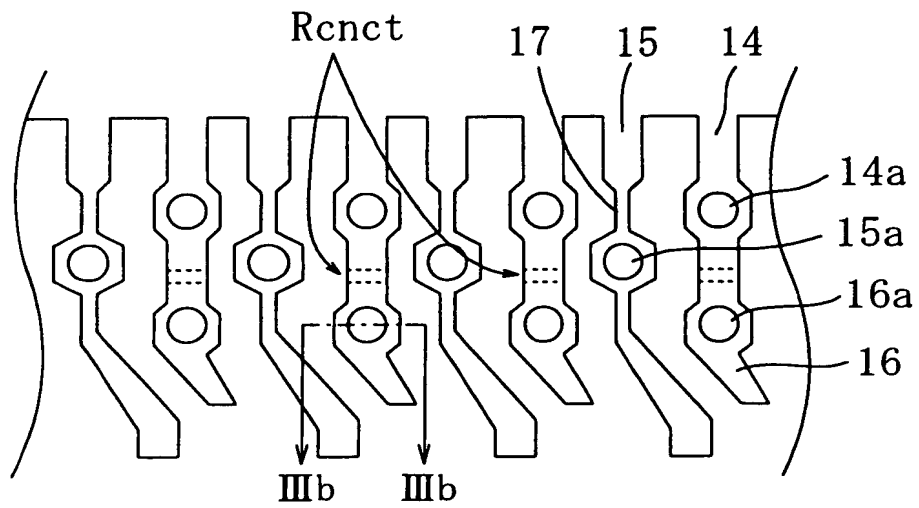


FIG. 3B

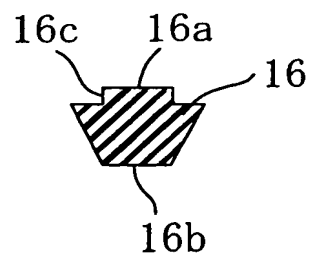


FIG. 4A

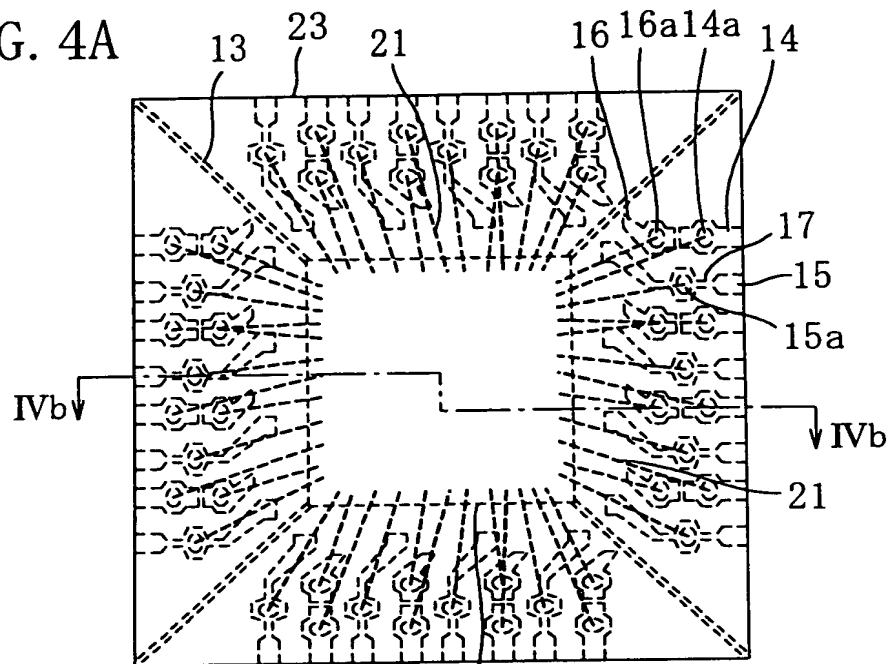


FIG. 4B

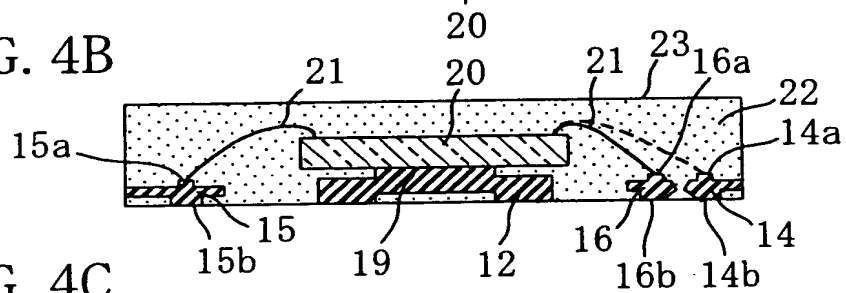
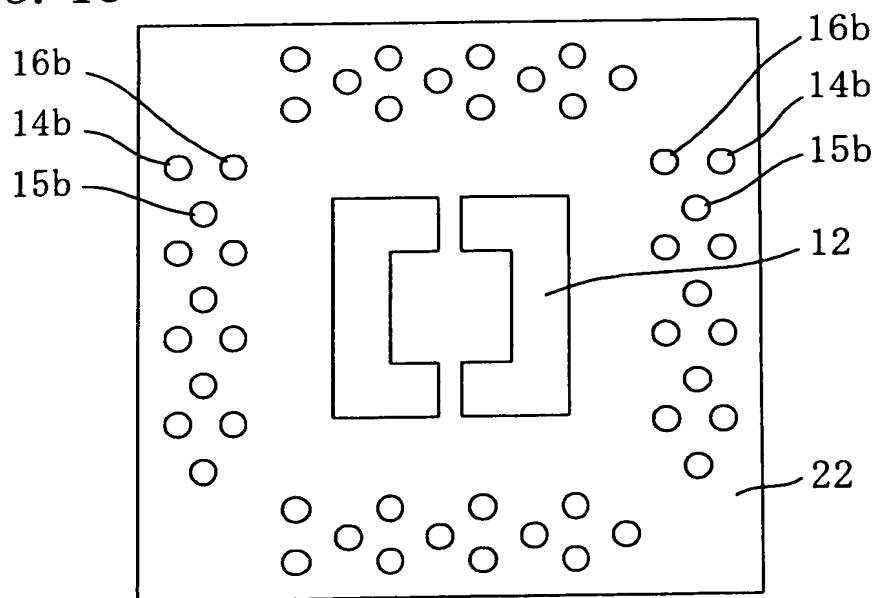


FIG. 4C



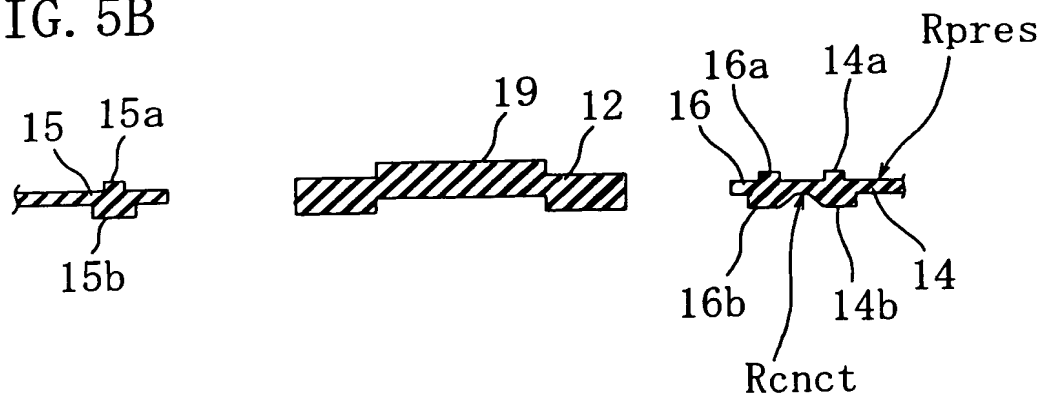


FIG. 6A

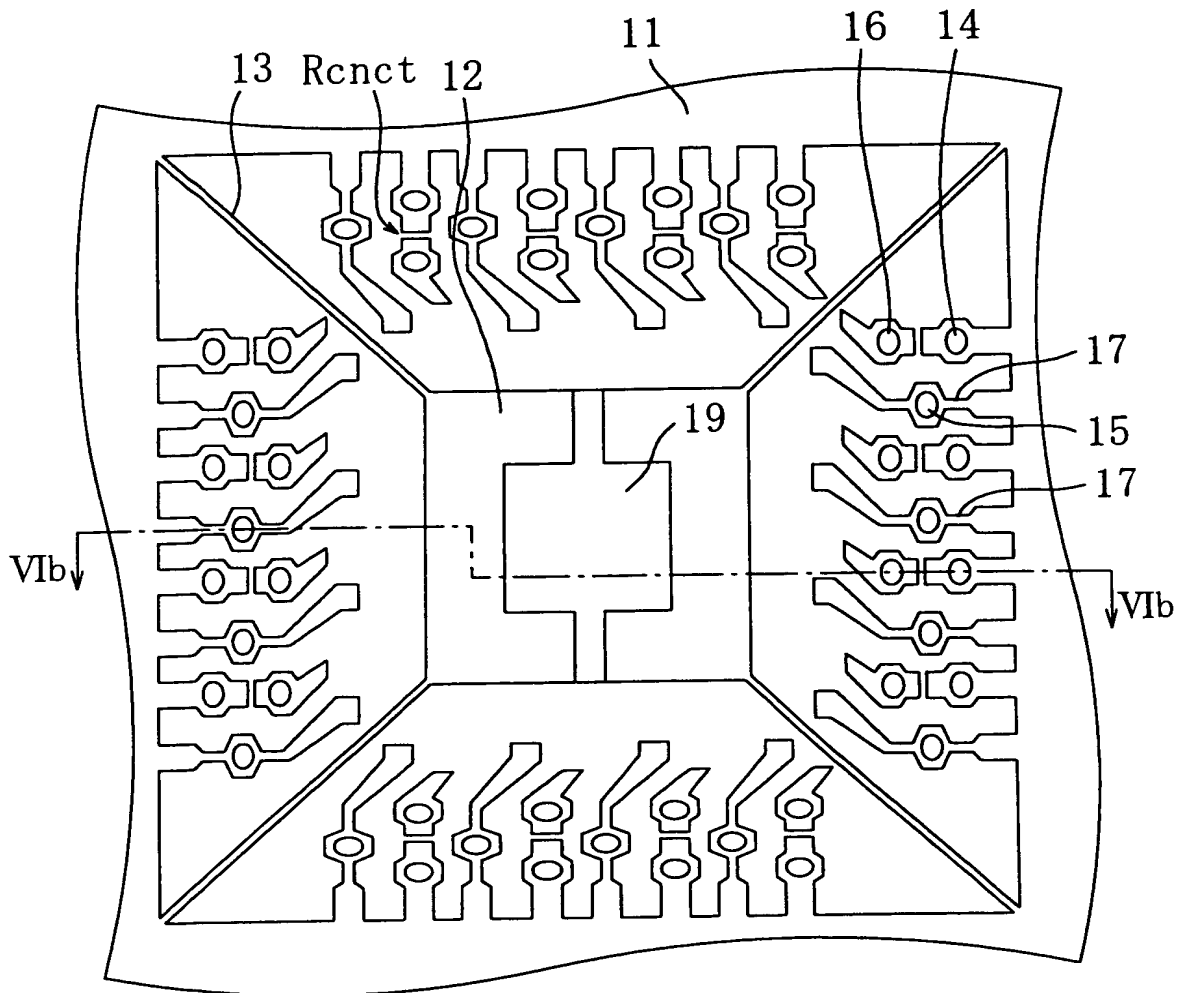


FIG. 6B

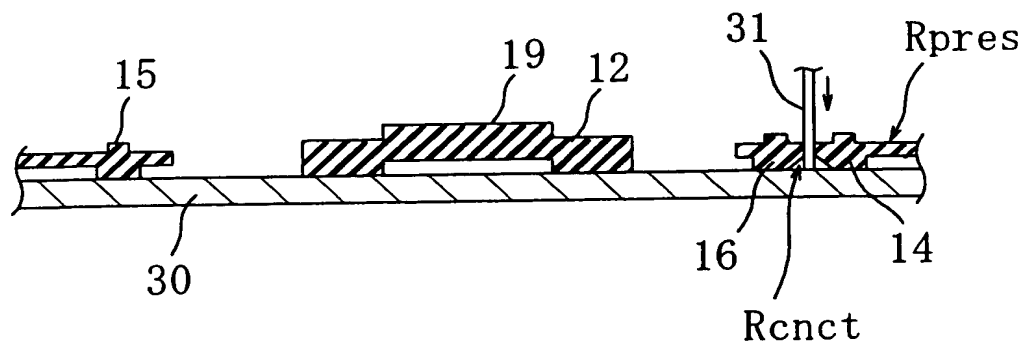


FIG. 7A

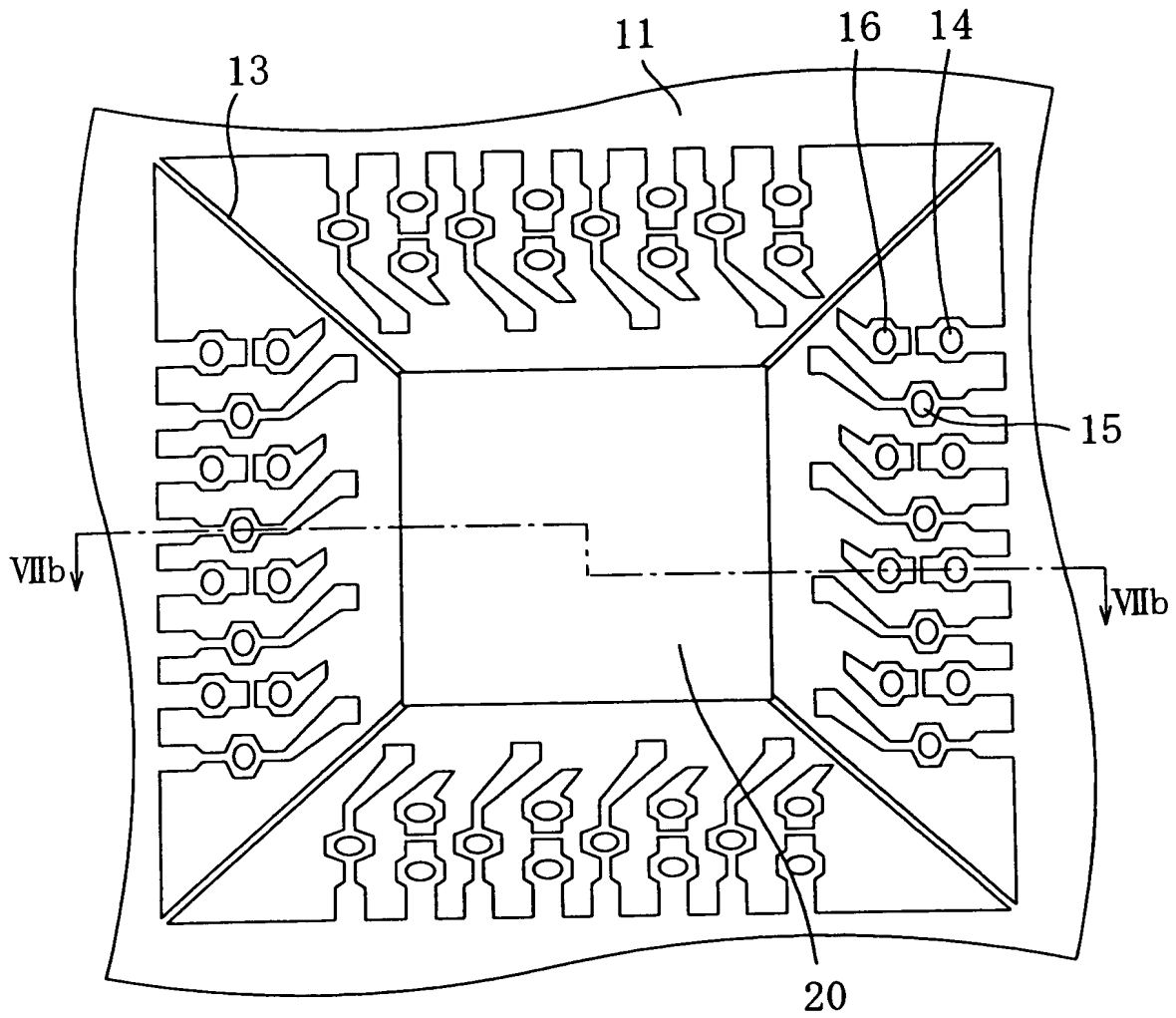


FIG. 7B

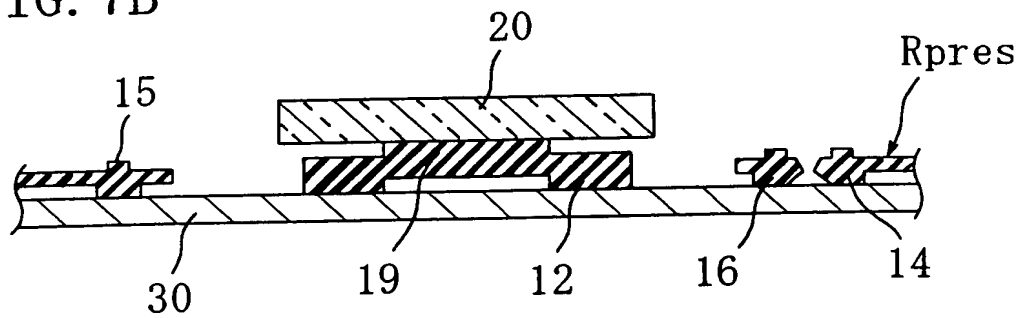


FIG. 8A

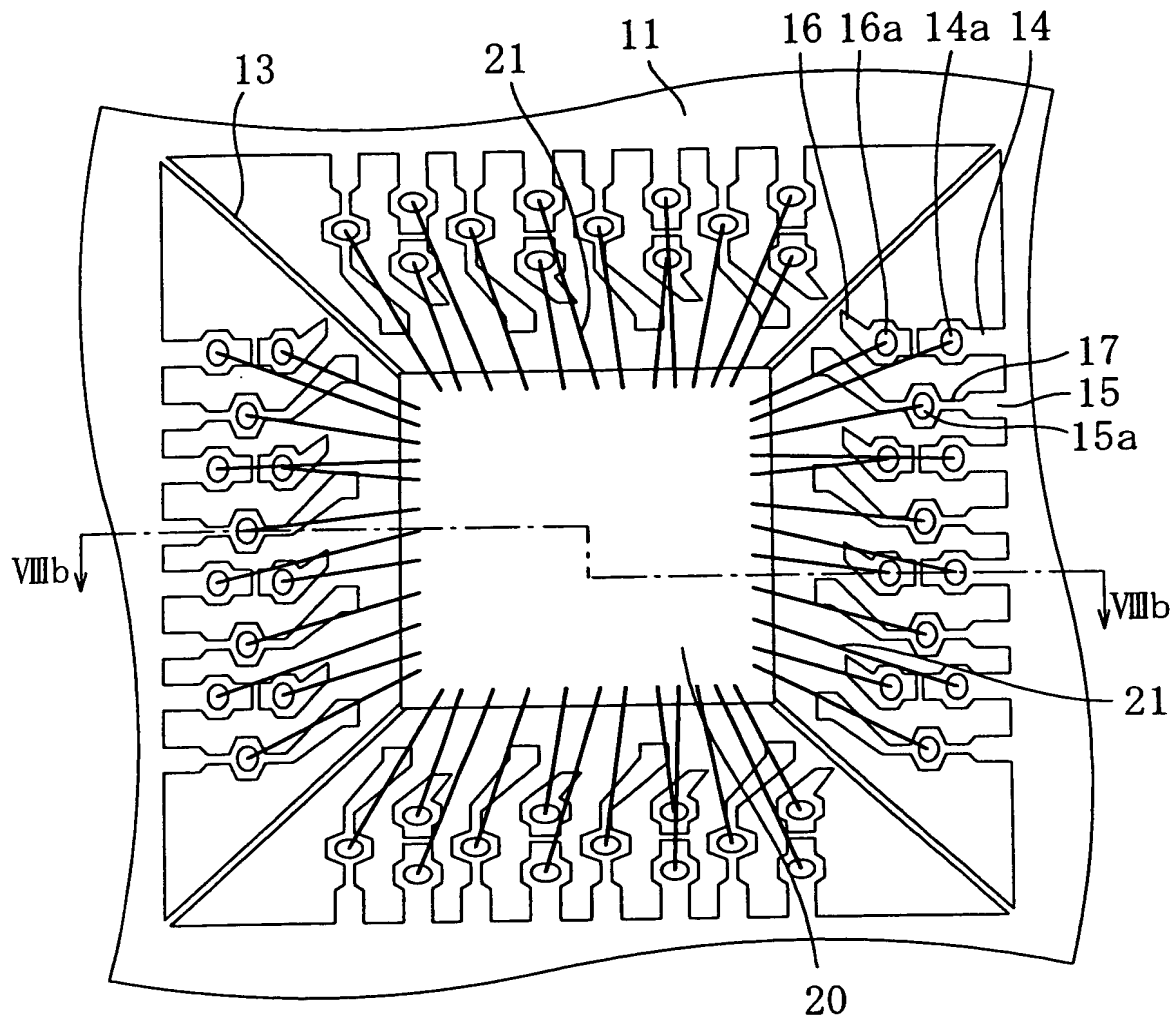


FIG. 8B

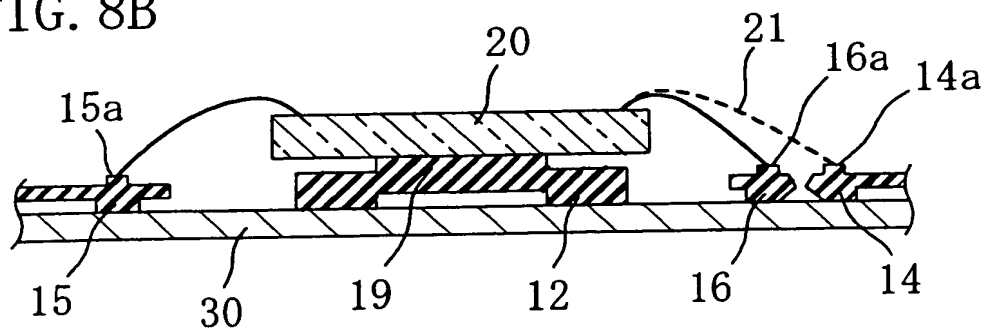


FIG. 9A

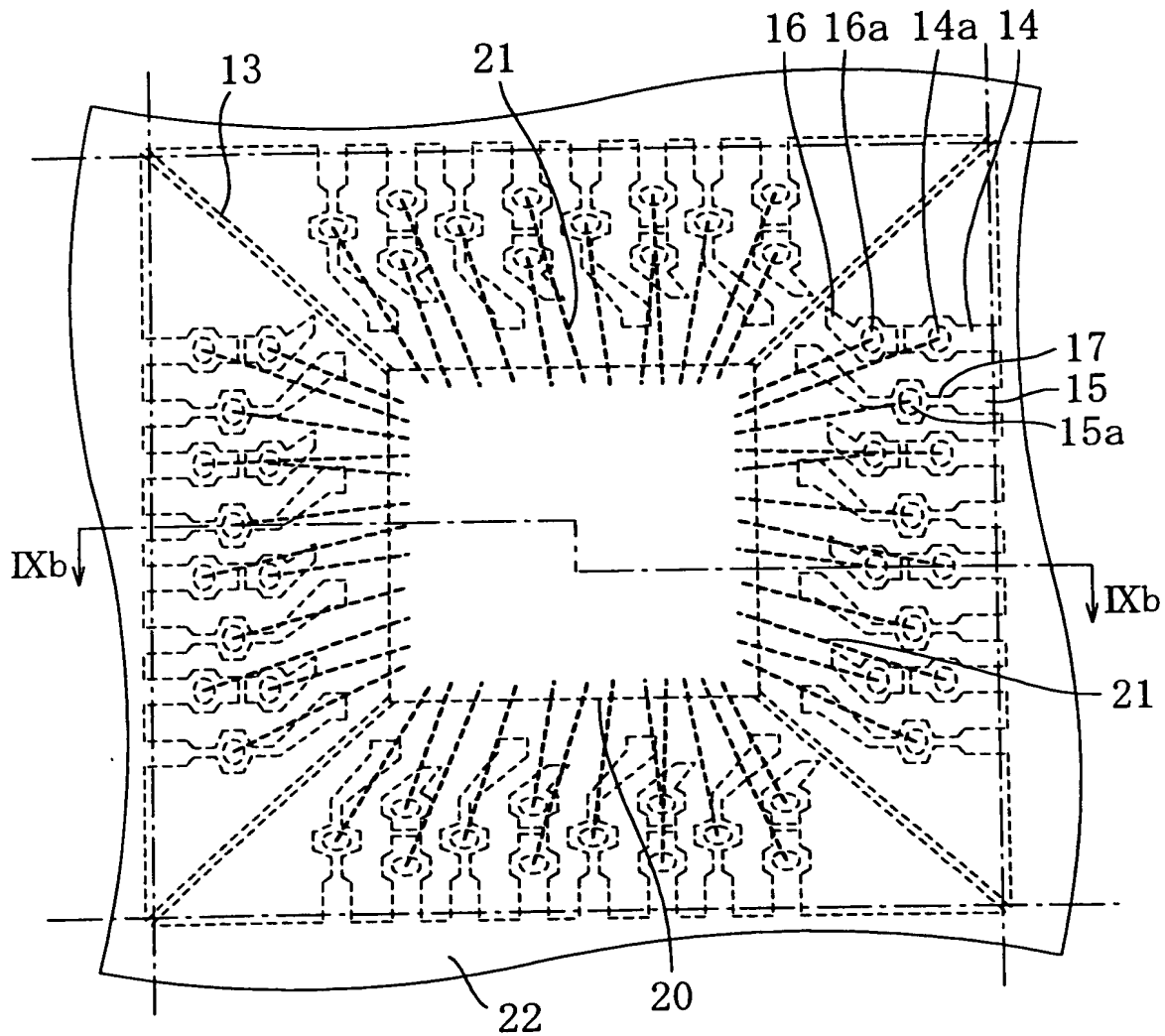


FIG. 9B

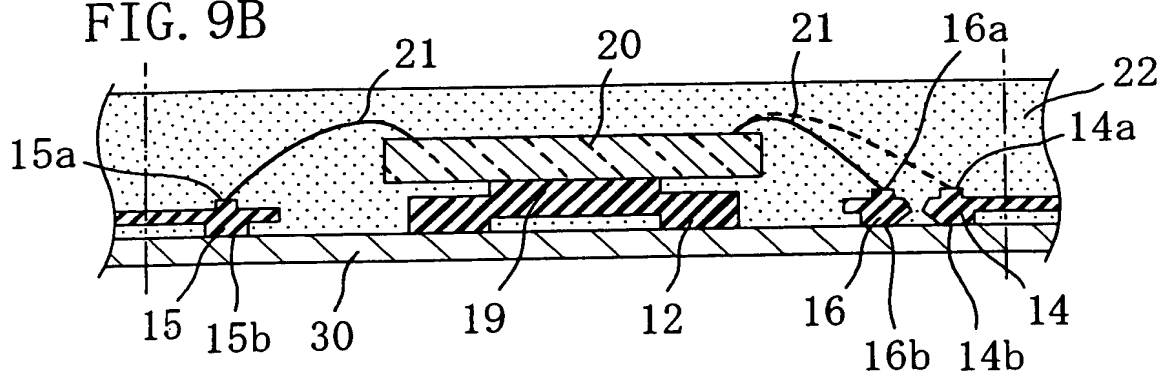


FIG. 10B

FIG. 10B is a cross-sectional view of a semiconductor device. It shows a substrate 20 with a top layer 21. A central region contains a structure 19 with a top layer 12. On the left, there is a structure 15 with a top layer 15a and a bottom layer 15b. On the right, there is a structure 16 with a top layer 16a and a bottom layer 16b. A dashed line 14a indicates a boundary or interface, and a solid line 14b indicates another boundary or interface. A region 22 is also labeled on the right side.

FIG. 11
PRIOR ART

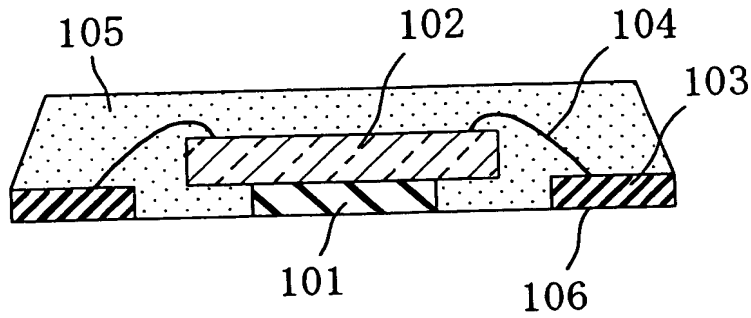


FIG. 12
PRIOR ART

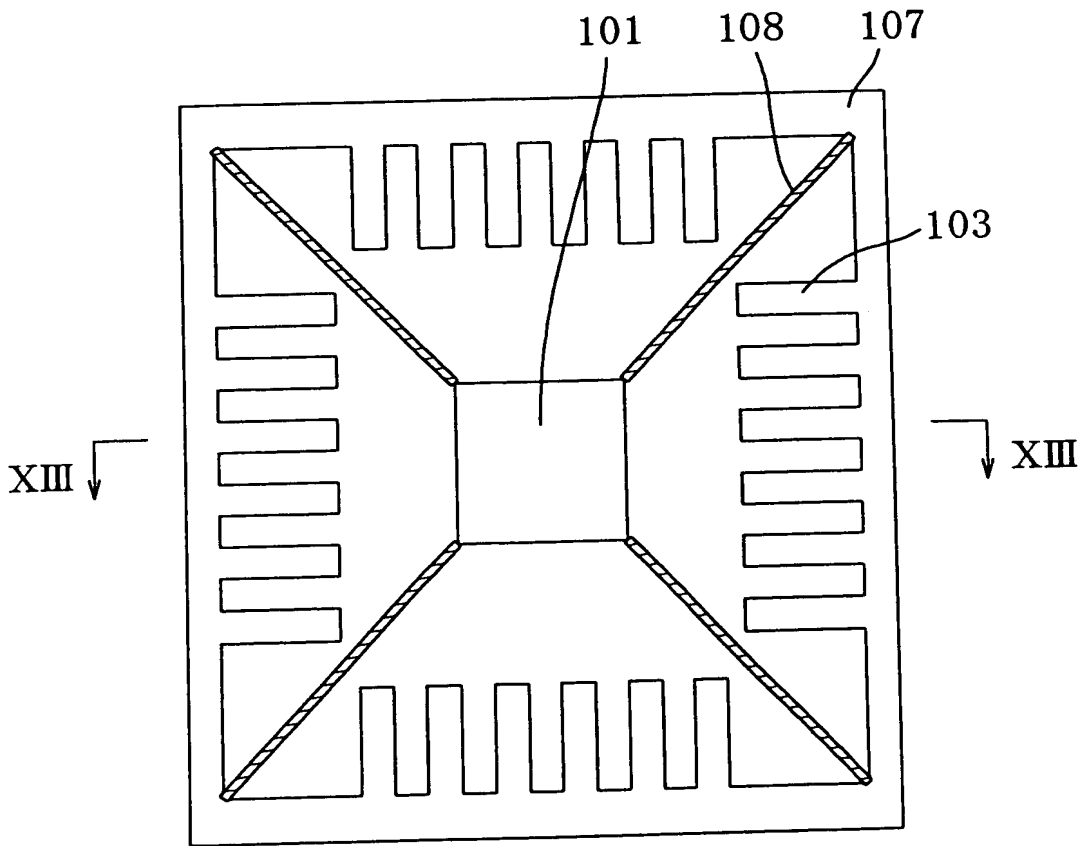




FIG. 13A

PRIOR ART

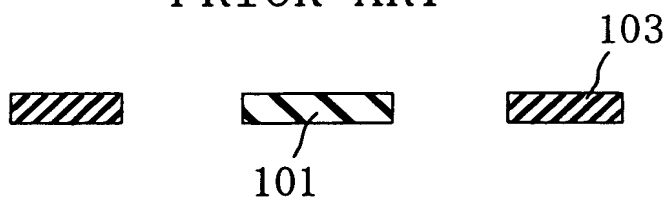


FIG. 13B

PRIOR ART

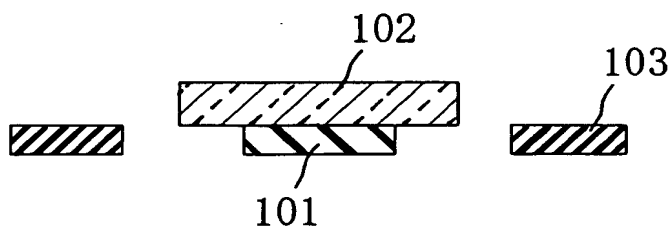


FIG. 13C

PRIOR ART

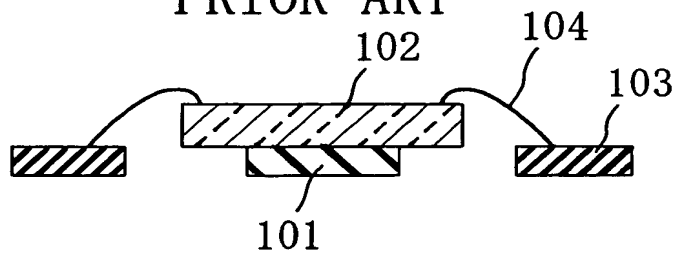


FIG. 13D

PRIOR ART

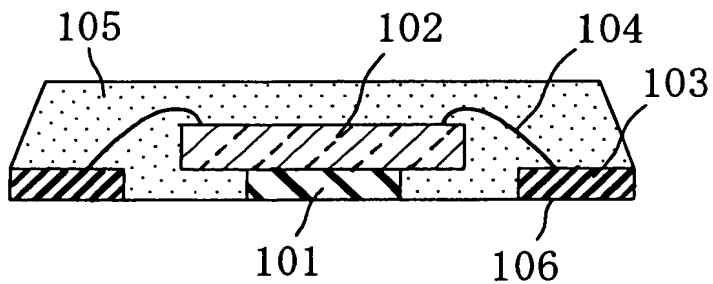




FIG. 14A
PRIOR ART

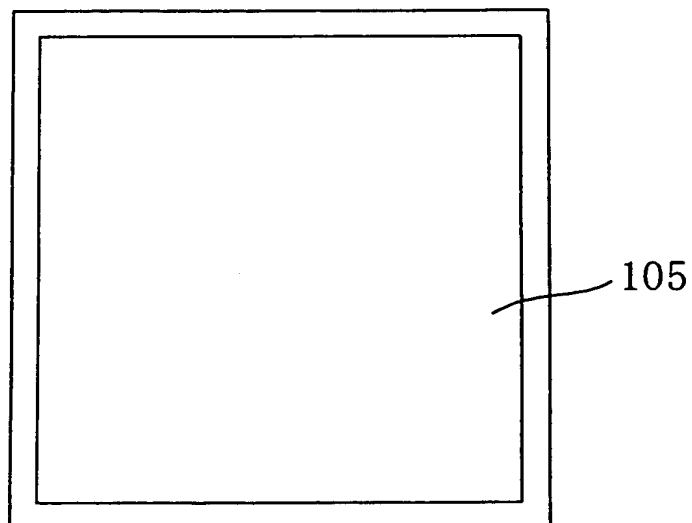


FIG. 14B
PRIOR ART

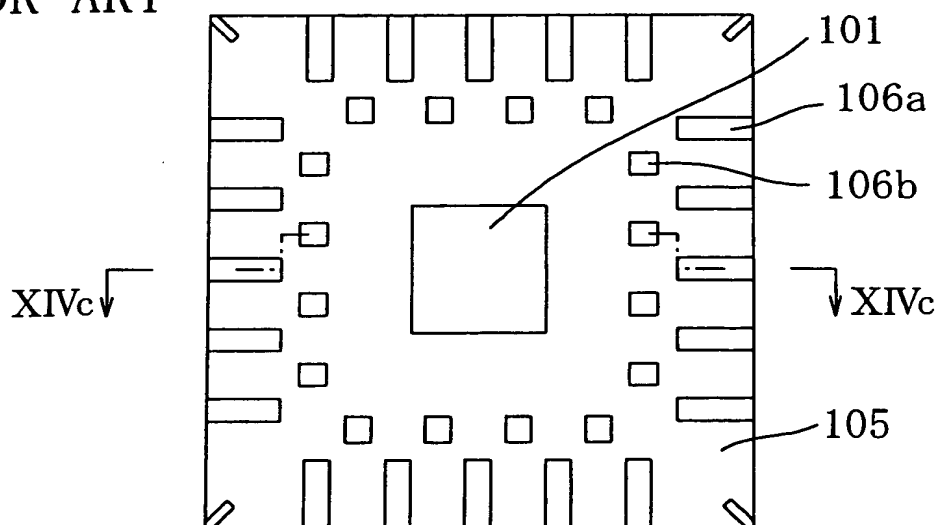


FIG. 14C
PRIOR ART

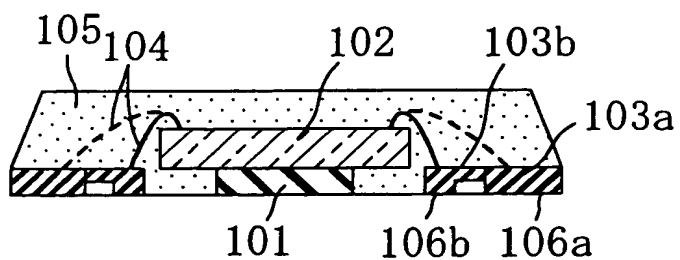




FIG. 15
PRIOR ART

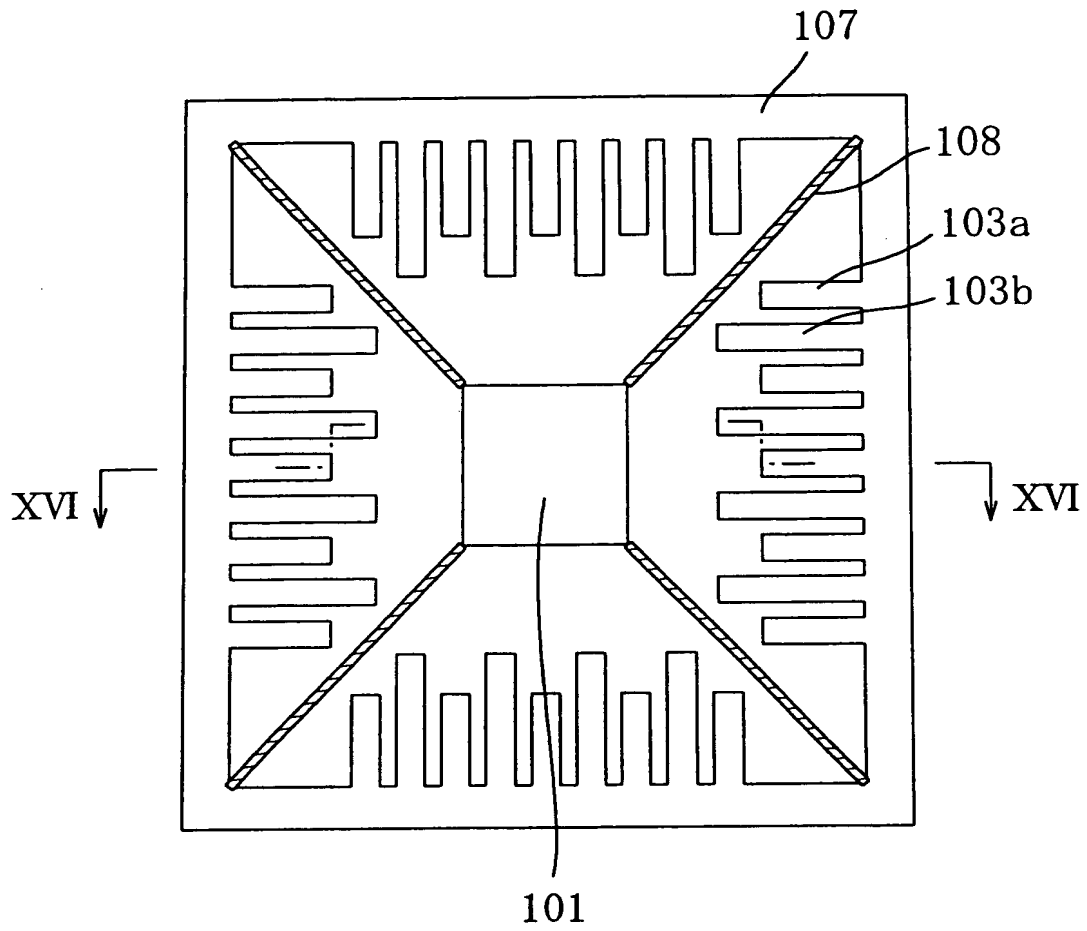


FIG. 16A

PRIOR ART

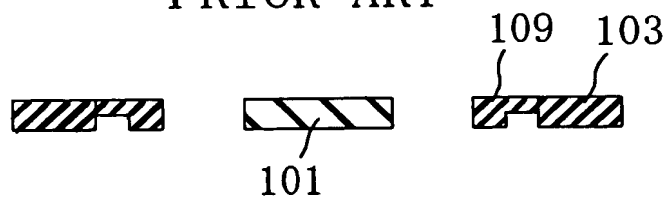


FIG. 16B

PRIOR ART

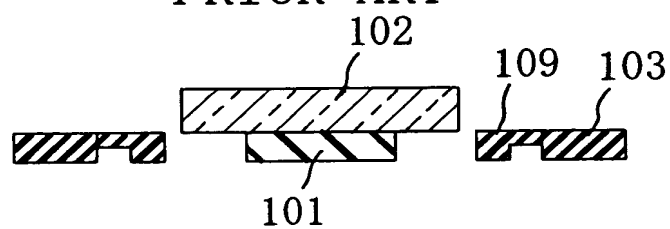


FIG. 16C

PRIOR ART

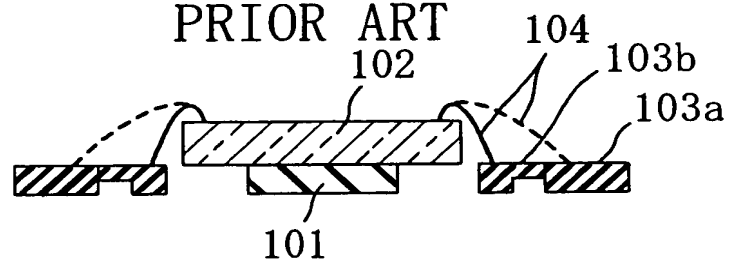


FIG. 16D

PRIOR ART

